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(54) High-speed digital accumulator with wide dynamic range

(57) A high-speed digital accumulator with wide dynamic range, the particularity whereof is the fact that it comprises a first adder stage (15), in which an input addend (X) is added to a value of a least significant part (11) of an accumulator at the preceding clock period, and at least one second stage, which comprises incrementer/decrementer means (18) suitable to perform an increment, decrement or identity operation on a most significant part of the accumulator, the incrementer/decrementer means further comprising logic means suitable to trigger an increment, a decrement or an identity of the most significant part on the basis of a decision made on results obtained at the previous clock period.

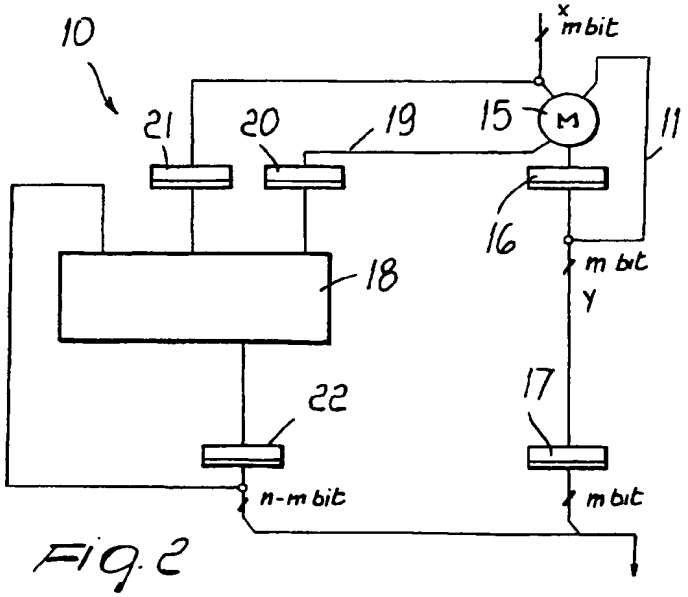

Fig. 2

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Description

[0001] The present invention relates to a high-speed digital accumulator with wide dynamic range. More particularly, the invention relates to a high-speed digital accumulator with wide dynamic range which uses a twos-complement digital adder.

[0002] It is known that digital accumulators consist of an adder which receives an input and the value of the accumulator itself in the preceding time period. In practice, the transfer function of said digital accumulators in Z-transforms is as follows:

$$Y = \frac{z}{z-1} \cdot X$$

[0003] Figure 1 illustrates a digital accumulator executed according to the prior art.

[0004] As shown in Figure 1, the accumulator thus comprises a digital adder 1, the input whereof receives an addend X which is m bits long and also receives the value of the accumulator during the preceding clock period; said value has a length of n bits, since the adder is an n-bit adder. In this case, the output datum Y has a length of n bits.

[0005] The reference numeral 2 designates an accumulation register for the result of the adder 1.

[0006] In this structure it is assumed that n is much larger than m.

[0007] The above-described structure has the drawback that it is inherently slow, since the sum performed by the adder 1 must be completed in a time which is short enough to satisfy the following relation:

$$T_{sum(n)} + T_{setup} < T_{clock}$$

[0008] The pass time of the n-bit adder 1 added to the setup time of the bank of the register 2 must be shorter than the clock time with which the structure is supplied.

[0009] Accordingly, it is sometimes difficult to satisfy the above relation, especially in high-speed applications, where it is not possible to use simple ripple-carry adders and therefore structures of the look-ahead or carry select type are used, always with the ultimate goal of satisfying the above equation.

[0010] The aim of the present invention is therefore to provide a high-speed digital accumulator with wide dynamic range which has a very large number of significant digits with respect to the operating frequency.

[0011] Within the scope of this aim, an object of the present invention is to provide a high-speed digital accumulator with wide dynamic range which allows to perform the operation of a digital accumulator in at least two clock cycles by means of a pipeline.

[0012] Another object of the present invention is to provide a high-speed digital accumulator with wide dynamic range which uses a high-speed, reduced-area twos-complement digital adder.

[0013] Another object of the present invention is to provide a high-speed digital accumulator with wide dynamic range which is highly reliable, relatively easy to manufacture and at competitive costs.

[0014] This aim, these objects and others which will become apparent hereinafter are achieved by a high-speed digital accumulator with wide dynamic range, characterized in that it comprises a first adder stage, in which an input addend is added to a value of a least significant part of an accumulator at the preceding clock period, and at least one second stage, which comprises incrementer/decrementer means suitable to perform an increment, decrement or identity operation on a most significant part of said accumulator, said incrementer/decrementer means further comprising logic means suitable to trigger an increment, a decrement or an identity of said most significant part on the basis of a decision made on results obtained at the preceding clock period.

[0015] Further characteristics and advantages of the invention will become apparent from the description of a preferred embodiment of the digital accumulator according to the invention, illustrated only by way of non-limitative example in the accompanying drawings, wherein:

Figure 1 is a block diagram of a conventional digital accumulator; and
Figure 2 is a block diagram of a digital accumulator executed according to the present invention.

[0016] Figure 1 was described earlier and therefore is not described further in this part of the description.

[0017] Accordingly with reference to Figure 2, the digital accumulator according to the present invention, generally designated by the reference numeral 10, comprises a digital adder 15 which receives in input an m-bit addend X and the output 11 of the adder, i.e., the value of the accumulator at the preceding time period, which is m bits long. A register 16 accumulates the result of the adder 15 and a register 17 accumulates in each instance the m bits in output from the digital adder 15.

[0018] The output of the register 17 is therefore again m bits long.

[0019] The second stage of the structure of Figure 2 provides for an increment, decrement or identity operation performed in incrementer/decrementer means 18 which receive in input the sign of the addend X, i.e., one bit; the incrementer/decrementer means 18 receive in input the overflow 19 in output from the adder 15, acquired at the preceding time period, and the most significant part of the accumulator y_1 acquired at the preceding period.

[0020] The incrementer/decrementer means 18 contain a truth table, on the basis of which a decision is

made to perform an increment, a decrement or an identity on the most significant part y_1 of the accumulator. The decision is made on the basis of the results of the preceding stage.

[0021] Additional registers 20 and 21 are provided to accumulate respectively the overflow 19 and the sign of the addend X.

[0022] Finally, a register 22 is provided in order to accumulate the most significant part y_1 of the accumulator.

[0023] The output of the register 22 has a length of m-n bits, which are combined with the m bits in output from the register 17. Accordingly, the output of the accumulator according to the invention has a total length of n bits.

[0024] The truth table contained in the incrementer/decrementer means 18 prescribes that if the sign of the addend X is equal to 1 at the preceding time period and the overflow at the same period is equal to 0, then the most significant part y_1 is decremented by 1; if instead the sign of the addend X at the preceding time period is 0 and the overflow 19 at the same period is 1, then the most significant part y_1 is equal to the most significant part y_1 at the preceding period, increased by 1.

[0025] If the sign of the addend X at the preceding time period is equal to 1 and the overflow 19 at the same period is 1, then the most significant part y_1 is equal to the most significant part at the preceding period; finally, if the sign of the addend X at the preceding time period is 0 and the overflow 19 calculated at the same period is equal to 0, then the most significant part is equal to the most significant part at the preceding time period.

[0026] In this manner, in the first stage of the accumulator according to the invention the input is added to the most significant part of the accumulator, while the second stage merely performs an increment/decrement operation, or neither of these, on the most significant part of the accumulator, on the basis of the outcome of a decision made according to the above-described truth table, in which the results acquired in the preceding stage are entered.

[0027] Accordingly, an accumulation with two clock cycles of latency is obtained, but the above-described equation is converted into the following pair of equations, where the addition time, in this case, is equal to the time of the decision made in the incrementer/decrementer means 18 plus the increment/decrement time also provided in the same means 18.

$$T_{sum(m)}+T_{setup}<T_{clock}$$

$$T_{decision}+T_{incdec(n-m)}+T_{setup}<T_{clock}$$

[0028] The operation of the accumulator depends only on one of the two preceding equations and particularly on the one that has the biggest first member.

[0029] Since m is much smaller than n, it is evident that it becomes possible to considerably increase the clock frequency without sacrificing anything in terms of number of significant digits.

[0030] In practice it has been observed that the digital accumulator according to the present invention fully achieves the intended aim and objects, since it allows to provide the transfer function of a digital accumulator in two or more clock cycles by means of a pipeline.

[0031] The accumulator thus conceived is susceptible of numerous modifications and variations, all of which are within the scope of the inventive concept.

[0032] Thus, for example, it is possible to extend the above-described structure by increasing the number of stages in the pipeline. In this manner it is possible to increase the bits in the most significant part of the accumulator without thereby having to reduce the clock frequency.

[0033] Finally, all the details may be replaced with other technically equivalent elements.

[0034] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly such reference signs do not have any limiting effect on the interpretation of each element identified by way of example by such reference signs.

Claims

1. A high-speed digital accumulator with wide dynamic range, characterized in that it comprises a first adder stage, in which an input addend is added to a value of a least significant part of an accumulator at the preceding clock period, and at least one second stage, which comprises incrementer/decrementer means suitable to perform an increment, decrement or identity operation on a most significant part of said accumulator, said incrementer/decrementer means further comprising logic means suitable to trigger an increment, a decrement or an identity of said most significant part on the basis of a decision made on results obtained at the preceding clock period.

2. An accumulator according to claim 1, characterized in that said first stage comprises a digital adder which receives in input said addend and the least significant part of said accumulator, acquired in the preceding clock period, in order to produce in output said least significant part.

3. An accumulator according to claim 2, characterized in that said incrementer/decrementer means receive in input the sign bit of said addend in input to the first adder stage, an overflow bit output by said adder and the most significant part of said accumulator; said sign bit, said overflow bit and said most significant part being determined at the

preceding clock period.

4. An accumulator according to one or more of the preceding claims, characterized in that the output of said incrementer/decrementer means which constitutes said most significant part of the accumulator is combined in output with said least significant part.

5. An accumulator according to one or more of the preceding claims, characterized in that said adder has a length which is equal to the bit length of said least significant part.

6. An accumulator according to one or more of the preceding claims, characterized in that if the sign bit of the input addend and said overflow bit have the same value, then said most significant part at the preceding clock period remains unchanged.

7. An accumulator according to one or more of the preceding claims, characterized in that if the sign bit of the input addend and said overflow bit have different values, then said most significant part at the preceding clock period is incremented by 1 if said overflow bit has the value 1.

8. An accumulator according to one or more of the preceding claims, characterized in that if the sign bit of the input addend and said overflow bit have different values, then said most significant part at the preceding clock period is decremented by 1 if said overflow bit has the value 0.

9. A method for high-speed digital accumulation with wide dynamic range, characterized in that it comprises the steps of:

performing, during a first clock cycle, a sum of an addend with a value of a least significant part of an accumulator at the preceding clock period;
performing, in at least one subsequent clock cycle, an increment, decrement or identity operation on a most significant part of said accumulator, depending on the outcome of a decision made on the basis of the values, acquired during said first clock cycle, of the sign of said addend and of the sum overflow; and
combining in output said least significant part with said most significant part of the accumulator.

10. A method according to claim 9, characterized in that it comprises a step which consists in determining, if the sign bit of the input addend and said overflow bit have different values, an increment by 1 of said most significant part at the first clock cycle if said overflow bit has the value 1.

11. A method according to claim 9, characterized in that it comprises a step which consists in determining, if the sign bit of the input addend and said overflow bit have different values, a decrement by 1 of said most significant part at the first clock cycle if said overflow bit has the value 0.

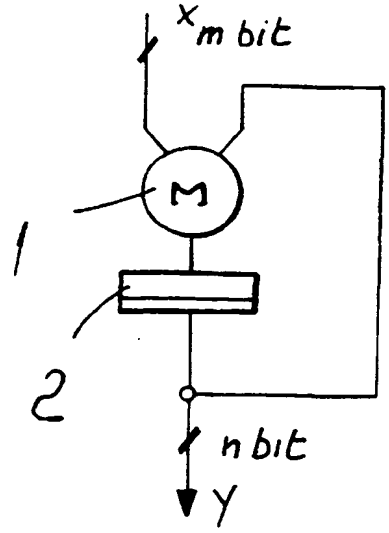

FIG. 1

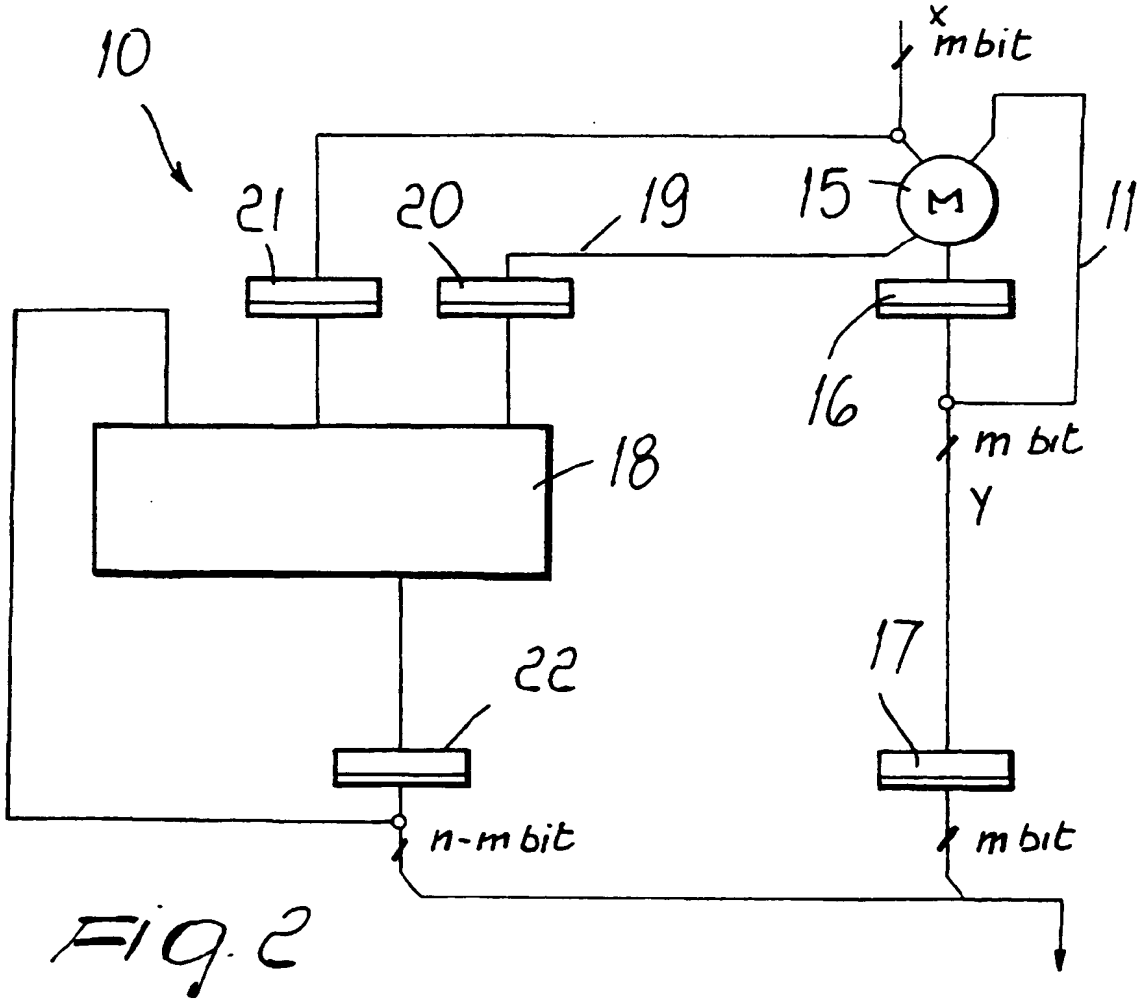

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0278

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 011, no. 207 (P-592), 4 July 1987 & JP 62 027864 A (PIONEER ELECTRONIC CORP), 5 February 1987 * abstract *	1-11	G06F7/50
X	KIRCHNER R ET AL: "ACCURATE ARITHMETIC FOR VECTOR PROCESSORS" NEW GENERATION COMPUTING, vol. 5, no. 3, June 1988, pages 250-270, XP000045065 * page 264, last paragraph - page 266, paragraph 1; figures 5,7 *	1-11	
X	A. CROISIER: "ACCUMULATOR FOR A DELTA TRANSVERSAL FILTER" IBM TECHNICAL DISCLOSURE BULLETIN., vol. 14, no. 10, March 1972, page 3120 XP002080193 NEW YORK US * the whole document *	1-8	
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 100 (P-561), 28 March 1987 & JP 61 250733 A (FUJITSU LTD), 7 November 1986 * abstract *	1-11	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06F
A	US 5 367 691 A (JOHNSON MARK J) 22 November 1994 * figure 1 *	1,9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 October 1998	Verhoof, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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